CMOS-Compatible Hybrid III-V/Si Photodiodes Using a Lateral Current Collection Scheme

Yannick Baumgartner\(^{1,2}\), Charles Caër\(^{1}\), Marc Seifried\(^{1}\), Gustavo Villares\(^{1}\), D. Caimi\(^{1}\), Thomas Morf\(^{1}\), Jérôme Faist\(^{2}\), Bert J. Offrein\(^{1}\), Lukas Czornomaz\(^{1}\)

\(^{1}\) IBM Research, Säumerstrasse 4, 8803 Rüschlikon, *umq@zurich.ibm.com
\(^{2}\) ETH Zurich, Institute of Quantum Electronics, Auguste-Piccard-Hof 1, 8093 Zürich

Abstract The CMOS-compatible front-end integration of ultra-compact lateral current collection III-V/Si photodetectors on a Silicon Photonics platform is demonstrated for the first time. The novel waveguide-coupled photodiodes show sub-nA dark current, ultra-low capacitance, a high responsivity, and data transmission at 25Gbps.

Introduction

Optical-interconnects based on silicon photonic integrated circuits (Si PICs) enable large bandwidth and cost-effective single-mode links, making them key candidates to handle the growing amount of data generated by modern communication applications, such as in cloud computing and storage systems\(^{1,2}\). Future Ethernet links will require data transmission exceeding 400 Gbps for a target power consumption of a few-J/bit at the photodetector level. To meet this demand, high-speed photodetectors (PDs) operating at datacom wavelengths are critical components of the link. PDs with ultra-low capacitance are required for high-speed and power-efficient operation. It implies a tight integration with electronics to minimize parasitic capacitances associated with the interconnection to the receiver circuit. Another advantage of ultra-low capacitance PDs resides in their integration with a high load resistance, which allows obtaining a sufficient output voltage for a sub-fJ optical input without using a trans-impedance amplifier (TIA)\(^{3}\).

High-speed PDs coupled to Si PICs were demonstrated with both germanium (Ge) and hybrid III-V/Si systems. Ge is a material of choice for Si PICs integrated PDs because it is more readily compatible with complementary metal oxide semiconductor (CMOS) processes and materials. State-of-the-art Ge PDs are typically grown by selective area growth on Si and can have bandwidth of 70 GHz and responsivity of 1 A/W at 1.55 \(\mu\)m\(^2\). However due to the small and indirect bandgap Ge PDs suffer from rather high dark currents and typically require a device length exceeding 10 \(\mu\)m to fully absorb the incoming light\(^4\). Owing to their tuneable and wider direct bandgap, heterogeneously-integrated III-V compounds have higher absorption coefficients and can then lead to ultra-compact and high-speed PDs with lower dark currents and increased efficiency in the O- and C-bands. While recent PDs were demonstrated using selective growth on Si\(^5\) the most performant waveguide-coupled PDs used a wafer bonding scheme\(^7-9\), where an InGaAs\(^7-10\) or a multi-quantum-well (MQW)\(^11,12\) (MQW) epitaxial stack is grown on an InP wafer and transferred on SOI waveguides by BCB or molecular bonding. Hybrid III-V/Si PDs with both a P-I-N or a modified uni-travelling-carrier\(^{14}\) (MUTC) architecture were proposed. However, the III-V/Si PDs shown so far did not use a viable integration path with CMOS technology.

In this work we report on the front-end integration of a novel waveguide-coupled high-speed III-V/Si PD providing independent optimization of Si to III-V light coupling, absorption length, carrier collection efficiency and speed. The PDs show sub-nA dark currents, ultra-low capacitances (~0.3-5.3 fF) and a device responsivity exceeding 0.5 A/W at V < -8 V. The PDs were tested for data communication and show an open eye at 25 Gbps.

Concept and fabrication

To minimize the parasitic capacitance associated with receiver circuits, we propose an integration of III-V PDs with CMOS electronics, where the III-
V is integrated between the front end of the line (FEOL) and the back end of the line (BEOL), as shown in Figure 1a. This way a common BEOL can be used for both the PICs and CMOS circuitry. This requires that ultra-thin III-V layers\textsuperscript{12,13} must be integrated. The PDs reported in this work are as thin as 300 nm.

The Si to III-V optical coupling design is depicted in Figure 1b. The PDs are butt-joint coupled to regrown InP tapers, where the optical mode is adiabatically coupled. Compared to evanescently-coupled PDs where varying the device length leads to a trade-off between a high responsivity and a high bandwidth, our coupling scheme is independent from the PD performance. To comply with the thickness budget required for front-end integration, we designed PDs using a lateral current collection (LCC) scheme which provides a decoupling between the light propagation and the carrier collection directions, combined with a strong optical confinement of the mode. We used an InAlGaAs MQW comprising compressively-strained quantum-well as absorbing medium. The LCC design provides the opportunity to optimize both the bandwidth and the modal overlap. In the LCC-PDs the compressive strain within the QW results in two-dimensional electron and hole gases with higher mobilities, favouring in-plane carrier collection and leading to a shorter transit-time (and thus higher bandwidth) compared to bulk InGaAs. The MQW bandgap is 0.88 eV, targeting an optimized absorption in the O-band and lower dark currents compared to bulk InGaAs or Ge. We maximized the modal overlap (and absorption) by growing a stack with 10 QWs. Figure 2 shows the process flow for fabricating the LCC-PDs. We first fabricated the Si PIC on a 4-inch SOI wafer, where the Si passive devices were ICP-etched. The Si PIC wafer was then cladded with SiOx and the oxide was planarized 100 nm above the Si waveguides (SWG) by chemical mechanical polishing. An epitaxial InAlGaAs quaternary stack including compressively-strained QWs was grown on an InP wafer by metal-organic chemical vapor deposition (MOCVD). We transferred the epitaxial InAlGaAs stack onto an SOI wafer by molecular wafer bonding, applying a thin Al2O3 layer as the bonding layer\textsuperscript{14}. The mesas were defined by dry etching with a Cl2-based chemistry in ICP-RIE. The width of the absorbing region was set to W = 0.7 μm and gives rise to a transit-time limited bandwidth larger than that of InGaAs-based PDs (which is ~ 40 GHz\textsuperscript{15}). Sn- and Zn-doped InP contact areas were selectively regrown with doping concentrations N\textsubscript{D} = 10\textsuperscript{19} and N\textsubscript{A} = 3-10\textsuperscript{18} cm\textsuperscript{-3} respectively. An additional InGaAs cap with N\textsubscript{A} = 5-10\textsuperscript{19} cm\textsuperscript{-3} was grown on the p-side to facilitate ohmic contact of the PDs. A final regrowth of intrinsic InP was performed for the adiabatic couplers. We used CMOS-compatible Mo/W contacts with a standard two-metal level BEOL\textsuperscript{13} followed by a rapid thermal anneal at 350°C.

Figure 3a shows a scanning electron microscopy (SEM) cross section from one of our PDs after the selective regrowth of the p-type contact area. As can be seen in the inset from Fig 3a, the contact overgrowth was engineered to maximize the mode confinement and minimize any detrimental p-InP free carrier absorption. Figure 3b shows how the light is first coupled from the SWG to the regrown InP taper and is then transferred to the LCC-PDs via a butt-joint interface.

**Measurements and results**

Figure 4a shows the current-voltage (IV) characteristics and the bias-dependent responsivity of a L = 5 μm long InAlGaAs LCC-PD. The dark current is as low as 0.2 nA at ~ 4 V, which is to the best of our knowledge, the lowest reported value for hybrid III/V-Si PDs and results from the wider bandgap of InAlGaAs. This low dark current value ensures a low shot noise.
responsivity was calculated after subtracting insertion losses from the Si grating coupler ($\lambda = 1260$ nm) and then includes losses in the adiabatic coupler and at the butt-joint interface. It exceeds 0.5 A/W at V < -8 V, which is very good considering the length of the device. This results from the high modal overlap with the 10 InAlGaAs QWs. Capacitance-voltage (CV) measurements were conducted on the devices and are summarized in Figures 4b and 4c. The capacitance of longer devices with similar architecture was measured (Fig. 4b) and based on the length-dependence, the capacitance of the LCC-PDs as well as the parasitic capacitance from the GSG pads are determined. As shown in Figure 4c the capacitance of LCC-PDs ranges from 0.3-5.3 fF at -5 V for devices with length 2-20 μm, well below the 20 fF parasitic capacitance from the tungsten pads (total contact area 3x75x700 μm²). Such low capacitance allows bypassing the TIA amplifier if the LCC-PDs are used with a high load resistance in the kΩ range. Given the pad parasitics, taking advantage of the ultra-small device capacitance is only possible for LCC-PDs monolithically integrated with CMOS electronics where parasitic capacitance can be reduced to a few fF.

To test data transfer with the fabricated LCC-PDs, we measured eye diagrams using an RF source as a clock to a bit pattern generator driving a lithium niobate Mach-Zender modulator (MZM), with a cut-off frequency of ~25 GHz. A DC-bias of -10 V was applied to the PDs through a bias tee and GSG RF probes. Figure 5 shows the eye patterns of a NRZ PRBS 2^7-1 signal, obtained at 10, 15 and 25 Gbps. The clear eye openings at high data-rates together with the ultra-low capacitance and dark current provides a direct evidence that the LCC-PDs are promising for high-speed single-mode links in datacentres.

Conclusions
We have successfully demonstrated the front-end integration of CMOS-compatible hybrid III-V/Si lateral current collection photodetectors on Silicon Photonics. The novel photodiode architecture and coupling scheme offer an advantageous design for strong optical confinement and the possibility to maximize both the bandwidth and the responsivity. The waveguide-coupled devices are ultra-compact and show a junction capacitance as low as 0.3 fF, allowing integration with a high load resistance instead of using a trans-impedance amplifier. The ultra-compact LCC-PDs demonstrate sub-nA dark current, a responsivity exceeding 0.5 A/W at V < -8 V and a clear eye opening when operated at 25 Gbps. This represents a milestone for on-chip optical interconnects with a high integration density and low power consumption.

Acknowledgements
We thank the MIND and Neuromorphic Devices and Systems Groups for fruitful discussions and the BRNC OpTeam for support. This project has received funding from the EU-H2020 research and innovation program under grants no. 688003 (DIMENSION), 688172 (ICT-STREAMS) and 688544 (L3MATRIX).

References