Novel CMOS-Compatible Ultralow Capacitance Hybrid III-V/Si Photodetectors Tested up to 32 Gbps NRZ

Y. Baumgartner\textsuperscript{1,2}, M. Seifried\textsuperscript{1}, C. Caer\textsuperscript{1}, P. Stark\textsuperscript{1}, D. Caimi\textsuperscript{1}, J. Faist\textsuperscript{2}, B.J. Offrein\textsuperscript{1}, L. Czornomaz\textsuperscript{1}

\textsuperscript{1}IBM Research, Säumerstrasse 4, 8803 Rüschlikon, Switzerland.
\textsuperscript{2}ETH Zurich, Institute of Quantum Electronics, Auguste-Piccard-Hof 1, 8093 Zurich, Switzerland.

Abstract: We demonstrate the monolithic integration of CMOS-compatible ultralow capacitance hybrid III-V/Si photodetectors and test these devices up to 32Gbps NRZ. The lateral photodiodes are suitable for ultrafast optical communication without using a transimpedance amplifier.


1. Introduction
The increasing internal traffic in data centers requires solutions for optical communication exceeding 400 Gbps or 1 Tbps [1,2]. High-speed photodetectors (PDs) operating at datacom wavelengths with ultralow power consumption are important components of every optical link. Signal integrity is key for high speed operation and can be achieved by tightly co-integrating ultra-small capacitance PDs with CMOS electronics in a monolithic fashion [3]. Such an integration scheme allows for bypassing the transimpedance amplifier (TIA) using a high load resistor [4], decreasing the power consumption of the receiver dramatically. So far high-performance CMOS-integrated PDs were only demonstrated using Germanium [3,5], usually resulting in devices with high dark currents and low absorption coefficients when operated in the telecom O-band. Recently we have demonstrated ultra-thin hybrid III-V/Si photodetectors that can be integrated between the front-end and the back-end of the line of a Si CMOS technology [6] paving the way towards integrated low capacitance photodiodes suitable for operation without TIA.

In this paper we report on our latest generation of waveguide-coupled hybrid III-V/Si photodiodes showing a flat RF response up to 35 GHz, ultralow capacitance, high responsivity and data transmission tested up to 32 Gbps NRZ without using digital signal processing. These devices are suitable for monolithic integration with electronics for ultrafast optical communication.

2. Concept and Fabrication
Owing to their direct and tunable bandgap, heterogeneously-integrated III-V based PDs can lead to lower dark currents, better thermal behavior and improved absorption coefficients compared to Ge-based PDs. We propose to use PDs using a lateral current collection (LCC) scheme which provides a decoupling between the light propagation and the carrier collection directions, combined with a strong optical confinement of the mode. It enables the use of numerous compressively-strained InAlGaAs multi-quantum-wells (MQW) enhancing lateral transport of holes while maintaining a good modal overlap. At the same time, the lateral current collection scheme allows to make very-thin PDs (< 250 nm) with ultralow capacitance suitable for monolithic integration on top of CMOS electronics sharing the same back-end.

![Fig. 1. (a) Schematic of the coupling scheme between the Si PIC platform and the LCC-PD, (b) Top view micrograph of an ultra-small LCC-PD, (c) schematic and (d) experimental cross section of a device.](image-url)
As shown in Figure 1a and 1b we use a coupling scheme based on regrown InP tapers. Because it is located outside the PD, such coupling scheme allows independent optimization of light coupling, absorption length, carrier collection efficiency and bandwidth. Fig 1b shows a top-view micrograph of one of our lateral current collection photodiodes (LCC-PDs). The dimensions of the absorbing region can be as small as 0.4 µm² (W × L = 200 nm × 2 µm), leading to an expected transit-time bandwidth exceeding 100 GHz (based on bulk InGaAs [7]) and a sub-fF capacitance. Figure 1c and 1d show a schematic and experimental cross section.

We fabricated a Si PIC by patterning a 4-inch SOI wafer. After cladding the Si passive devices with SiO₂ and planarizing the oxide we transferred an epitaxial InAlGaAs stack onto the Si PIC by molecular wafer bonding. A compressively-strained MQW structure was chosen as absorbing medium, targeting an optimal absorption in the O-band and a reduced transit time due to the improved hole mobility. With the lateral architecture of the PDs, the modal overlap was maximized by growing a stack with 10 QWs. n- and p-InP contact areas were selectively regrown on the sides of the absorbing medium. Additional selective regrowth steps with highly-doped InGaAs and undoped InP were performed to respectively provide ohmic contact to p-InP and low-loss adiabatic couplers. The overall monolithic integration is achieved using CMOS-compatible fabrication processes and Mo/W ohmic contacts [8,9].

3. DC and RF characterization

Figure 2a shows the IV characteristics of a lateral current collection photodetector at 25 °C and 85 °C. The ultralow dark current (0.4 nA at −4 V) is a consequence of the wider bandgap of our InAlGaAs absorbing medium and ensures a low shot noise. When raising the temperature to 85°C the dark current only increases by one order of magnitude, still much lower compared to typical values from Ge-based PDs [10]. As can be seen in Figure 2b the capacitance of LCC-PDs ranges from 0.3-2.5 fF at -5 V for devices with length 2-10 µm. This exceptionally low device capacitance is a direct consequence of the lateral architecture of our devices but requires the LCC-PD to be monolithically integrated with electronics, to reduce the interconnect parasitic capacitance to a few fF. Ultimately the integration of LCC-PDs with a load resistor in the kΩ range, replacing the use of a TIA, can further reduce the energy consumption per bit, both by reducing the energy consumption and the interconnect parasitic capacitance.

![Figure 2](image-url)

**Fig. 2.** (a) Temperature dependence of the dark current and responsivity of an LCC-PD, (b) Device capacitance as a function of the device length.

Fig 2a shows the responsivity of a LCC-PD, exhibiting similar DC responsivity as our previously-reported devices. This is a result of the high modal overlap with the 10 QWs. However, our former devices suffered from a low RF responsivity (< 0.15 A/W) which was the result of a non-optimal optical design where most of the responsivity originated from slow carriers. This new generation of devices now provides similar responsivity at high frequencies.

Figure 3a shows an optical image of a LCC-PD under test. Figure 3b depicts a comparison of the frequency response of our old and improved LCC-PD design. As mentioned above, we drastically improved our RF responsivity resulting in a 3dB bandwidth beyond our measurement capabilities (25-30 GHz, limited by the modulator). To test data transmission with the fabricated LCC-PDs, we measured eye diagrams using a bit pattern generator driving a lithium niobate Mach-Zender modulator, with a cut-off frequency of ~25 GHz. Figure 3c shows the obtained eye diagrams of a non-return-to-zero (NRZ) pseudo random binary sequence (PRBS) 2^7-1 signal, obtained at 20, 25 and 32 Gbps and acquired without any pre-emphasis.
Fig. 3. (a) Optical image of the LCC-PD under test, (b) Frequency response of LCC-PDs with new and old design (V = -8V), (c) Eye diagrams at 20, 25 and 32 Gbps NRZ (V = -10V, no pre-emphasis, 20 ps/div, 10 mV/div).

3. Conclusions

We achieved record low dark current, ultralow capacitance, a flat RF response up to 35 GHz and demonstrated 32 Gbps NRZ transmission with our novel CMOS-compatible hybrid III-V/Si lateral current collection photodetectors. These devices are suitable for monolithic integration with electronics, paving the way towards integrated low capacitance photodiodes suitable for operation without TIA. It will provide drastic improvement in the link energy budget, targeting 400GbE optical communication.

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5. References


